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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/953,719	10/17/1997	DAISUKE YOSHIDA	35.C12338	4164

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EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 02/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/953,719	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-19,21,22,24-38 and 49-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-19,21,22,24-38 and 49-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 1997* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 27, 2002 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5, 7-12, 15, 16, 18, 19, 21, 22, 24-29, 32, 33, 35, 38, and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (US 5,589,847) in view of Yamaguchi (US 5,438,342) and Shinya (US 5,170,158).

In regards to claim 1, Lewis discloses a matrix substrate having switching elements (transistors) connected to picture element electrodes (550), intersecting scanning (G) and signal lines (D), an input terminal for inputting digital video data (i.e. "Digital data in"), a circuit (505) changing an initial sequencing order of the digital video data inputted through the input terminal into a different sequencing order, and for outputting the digital video data in the different

sequencing order, a digital horizontal scanning circuit (505) for sampling the digital video data in the initial sequencing order (wherein data for a complete line is transferred in parallel to latch circuitry), a latch circuit (515), a D/A converter (255), signal transfer switches (520), and transfer switch selection (i.e. select) for selecting at least one of the signal transfer switches to output analog signals in the same order as the different sequencing order of the digital video data [see Figures 15A-B; Column 10, Lines 22-35]; wherein a number M (M = 3) of the D/A converters is less than a number N (N = 12) of the switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of the M D/A converters to N/M (N/M = 12/3 = 4) plural switching elements (Fig. 15A; transistors connected to $D_{1\text{-}4}$, $D_{5\text{-}8}$, and $D_{9\text{-}12}$) arranged in a horizontal direction [see Column 10, Lines 36-48]. Lewis does not expressly disclose inverting the polarity of the analog signal from the D/A converter, nor a buffer disposed between the D/A converter and the selection circuit.

However, Yamaguchi discloses inverting analog signal polarity [Figure 1; Column 2, Lines 1-29]. Furthermore, Shinya discloses buffering (16 & 17) D/A converter (15) output [Fig. 2; Column 4, Lines 1-27]. Lewis, Shinya and Yamaguchi are analogous art because they are from the field of driving matrix displays. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to utilize Yamaguchi's analog signal inversion and Shinya's buffers with Lewis' analog data signals to suppress flicker and crosstalk.

In regards to claim 2, Lewis discloses applying analog signals to the signal lines (D) through the transfer switches (520) in every output of the selection circuit [see Figure 15B; Column 10, Lines 22-48].

In regards to claim 4, Lewis discloses a shift register (505) [see Figure 15A; Column 10, Lines 22-48].

In regards to claim 5, Lewis discloses a CMOS transistor for the switching element (550) [see Figure 15A; and the Abstract].

In regards to claim 7, Lewis discloses a D/A converter capable of inputting one bit more than the bit number of the picture data bits [see Figure 10; Column 8, Line 41 - Column 9, Line 10].

In regards to claim 8, Lewis discloses a changeover switch for selecting one of at least two groups of signal transfer switches (520) [see Figure 15A; Column 10, Lines 22-48].

In regards to claim 9, Lewis discloses supplying the picture data in divisions, and sampling is conducted by the horizontal scanning circuit (505) [see Figure 15B; Column 10, Lines 22-48].

In regards to claim 10, Lewis discloses changeover of the divided picture data [see Figure 10; Column 8, Line 54 - Column 9, Line 10].

In regards to claim 11, Lewis discloses an elevation circuit for boosting output [see Figures 3A-C; Column 6, Lines 37-56].

In regards to claim 12, Lewis discloses a clamp type amplifier [see Figures 3A-C; Column 6, Lines 37-56].

In regards to claim 15, Lewis discloses at least two analog buffer circuits and a circuit for selecting one of the buffer circuits [see Figure 10; Column 8, Line 54 - Column 9, Line 10].

In regards to claim 16, Lewis discloses positive and negative polarity [see Figure 10; Column 8, Line 54 - Column 9, Line 10].

In regards to claim 18, Lewis discloses a liquid crystal device comprising a matrix and a counter substrate having switching elements connected to picture element electrodes (550), intersecting scanning and signal lines (G) and signal lines (D), an input terminal for inputting digital video data (i.e. "Digital data in"), a circuit (505) for changing an initial sequencing order of the digital video data inputted through the input terminal into a different sequencing order, and for outputting the digital video data in the different sequencing order, a digital horizontal scanning circuit (505) for sampling the digital video data in the initial order (wherein data for a complete line is transferred in parallel to latch circuitry), a digital horizontal scanning circuit (505), a latch circuit (515), a D/A converter (255), signal transfer switches (520), and transfer switch selection (i.e. select) for selecting at least one of the signal transfer switches to output

analog signals in the same order as the different sequencing order of the digital video data [see Figures 15A-B; Column 10, Lines 22-35]; wherein a number M (M = 3) of the D/A converters is less than a number N (N = 12) of the switching elements arranged in a horizontal direction, and analog signals are sequentially inputted from particular ones of the M D/A converters to N/M (N/M = 12/3 = 4) plural switching elements (Fig. 15A; transistors connected to $D_{1\text{-}4}$, $D_{5\text{-}8}$, and $D_{9\text{-}12}$) arranged in a horizontal direction [see Column 10, Lines 36-48]. Lewis does not expressly disclose means for inputting signal-polarity inverting signals together with the picture data, nor for inverting the polarity of the analog output of the D/A converter, nor a buffer disposed between the D/A converter and the selection circuit.

However, Yamaguchi discloses inverting analog signal polarity [Figure 1; Column 2, Lines 1-29]. Furthermore, Shinya discloses buffering (16 & 17) D/A converter (15) output [Fig. 2; Column 4, Lines 1-27]. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to utilize Yamaguchi's analog signal inversion and Shinya's buffers with Lewis' analog data signals to suppress flicker and crosstalk.

In regards to claim 19, Lewis discloses applying analog signals to the signal lines (D) through the transfer switches (520) in every output of the selection circuit [see Figure 15B; Column 10, Lines 22-48].

In regards to claim 21, Lewis discloses a shift register (505) [see Figure 15A; Column 10, Lines 22-48].

In regards to claim 22, Lewis discloses a CMOS transistor for the switching element (550) [see Figure 15A; and the Abstract].

In regards to claim 24, Lewis discloses a D/A converter capable of inputting one bit more than the bit number of the picture data bits [see Figure 10; Column 8, Line 41 - Column 9, Line 10].

In regards to claim 25, Lewis discloses a changeover switch for selecting one of at least two groups of signal transfer switches (520) [see Figure 15A; Column 10, Lines 22-48].

In regards to claim 26, Lewis discloses supplying the picture data in divisions, and sampling is conducted by the horizontal scanning circuit (505) [see Figure 15B; Column 10, Lines 22-48].

In regards to claim 27, Lewis discloses changeover of the divided picture data [see Figure 10; Column 8, Line 54 - Column 9, Line 10].

In regards to claim 28, Lewis discloses an booster circuit for boosting output [see Figures 3A-C; Column 6, Lines 37-56].

In regards to claim 29, Lewis discloses a clamp type amplifier [see Figures 3A-C; Column 6, Lines 37-56].

In regards to claim 32, Lewis discloses at least two analog buffer circuits and a circuit for selecting one of the buffer circuits [see Figure 10; Column 8, Line 54 - Column 9, Line 10].

In regards to claim 33, Lewis discloses positive and negative polarity [see Figure 10; Column 8, Line 54 - Column 9, Line 10].

In regards to claim 35, Lewis discloses a display apparatus [see Column 1, Lines 9-17].

In regards to claim 38, Lewis does not expressly disclose a buffer connected to an output of the D/A converter. However, Yamaguchi discloses inverting analog signal polarity [Figure 1; Column 2, Lines 1-29]. Furthermore, Shinya discloses buffering (16 & 17) D/A converter (15) output [Fig. 2; Column 4, Lines 1-27]. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of the invention, to utilize Yamaguchi's analog signal inversion and Shinya's buffers with Lewis' analog data signals to suppress flicker and crosstalk.

In regards to claim 49, Lewis discloses a horizontal circuit comprising: an input terminal (see Fig. 15A, "Digital data in") for inputting digital video data; a sequencing circuit (see Fig. 15A, 505) for changing an initial sequencing order of the digital video data inputted through the input terminal into a different sequencing order, and for outputting the digital video data in the different sequencing order; a horizontal scanning circuit (see Fig. 15A, 505) for sampling the digital video data in the initial sequencing order (wherein data for a complete line is transferred

in parallel to latch circuitry); a latch circuit (see Fig. 15A, 515) for latching the sequenced digital video data synchronously with output from the horizontal scanning circuit; a D/A converter (see Fig. 15A, 255) for converting the digital video data output from the latch circuit into analog signals; plural signal transfer switches (see Fig. 15A, 520) provided between the D/A converter and plural signal lines (see Fig. 15A, "D"); and a transfer switch selection circuit (see Fig. 15A, 520) for selecting at least one of the plurality of signal transfer switches (see Fig. 15A, 550) to output the analog signal in the same order of the different sequencing order of the digital video data [see Fig. 15B and Column 10, Lines 22-48].

In regards to claim 50, Lewis discloses a shift register (Fig. 15A, 505) [see Column 10, Lines 22-48].

In regards to claim 51, Lewis discloses using a CMOS transistor for a signal transfer switch (Fig. 15A, 550) [see the Abstract].

4. Claims 13, 14, 17, 30, 31, 34, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis (5,589,847), Yamaguchi (5,438,342) and Shinya (5,170,158) as applied to claims 1, 18 and 35 above, and further in view of Misawa et al. (5,250,931).

In regards to claim 13, Lewis does not expressly disclose decoding signals.

However, Misawa et al. discloses decoding signals [see Figure 1; Column 4, Line 58 - Column 5, Line 5]. Lewis and Misawa et al. are analogous art because they are from the shared field of active matrix display technology.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to utilize Misawa's decoder in Lewis' driving circuit. The motivation for doing so would have been to provide a precise method of processing input signals. Therefore, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 13.

In regards to claim 14, Lewis does not expressly disclose a diffusion layer in a semiconductor substrate, and an impurity concentration of a diffusion layer.

However, Misawa et al. discloses a diffusion layer in a semiconductor substrate, and an impurity concentration of a diffusion layer [see Figures 3A-B; Column 6, Line 29 - Column 7, Line 59].

At the time of invention, it would have been obvious to a person of ordinary skill in the art to utilize Misawa's semiconductor substrate in Lewis' driving circuit. The motivation for doing so would have been to provide an inexpensive and accurate method of manufacturing the device. Therefore, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 14.

In regards to claim 17, Lewis does not expressly disclose polishing the picture element electrode by chemical mechanical polishing.

However, Misawa et al. discloses chemical mechanical polishing [see Figures 4A-D; Column 7, Line 60 - Column 8, Line 2].

At the time of invention, it would have been obvious to a person of ordinary skill in the art to utilize Misawa's polishing technique on Lewis' picture elements. The motivation for doing

so would have been to provide an inexpensive and precise method of producing the device. Therefore, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 17.

In regards to claim 30, Lewis does not expressly disclose decoding signals.

However, Misawa et al. discloses decoding signals [see Figure 1; Column 4, Line 58 - Column 5, Line 5].

For the reasons set forward in the above rejection of claim 13, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 30.

In regards to claim 31, Lewis does not expressly disclose discloses a diffusion layer in a semiconductor substrate, and an impurity concentration of a diffusion layer.

However, Misawa et al. discloses a diffusion layer in a semiconductor substrate, and an impurity concentration of a diffusion layer [see Figures 3A-B; Column 6, Line 29 - Column 7, Line 59].

For the reasons set forward in the above rejection of claim 14, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 31.

In regards to claim 34, Lewis does not expressly disclose polishing the picture element electrode by chemical mechanical polishing.

However, Misawa et al. discloses chemical mechanical polishing [see Figures 4A-D; Column 7, Line 60 - Column 8, Line 2].

For the reasons set forward in the above rejection of claim 17, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 34.

In regards to claim 36, Lewis does not expressly disclose a reflection type liquid crystal panel as the LCD.

However, Misawa et al. discloses a reflection type liquid crystal panel as the LCD, and displays a picture image by introducing light emitted from a light source to the liquid crystal panel, and projecting reflected light through an optical system onto a screen [see Figures 16-18; Column 15, Line 52 - Column 17, Line 34].

At the time of invention, it would have been obvious to a person of ordinary skill in the art to utilize Misawa's reflection type liquid crystal panel as Lewis' LCD. The motivation for doing so would have been to allow Lewis' device to drive a type of LCD with a large consumer market. Therefore, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 36.

In regards to claim 37, Lewis does not expressly disclose a liquid crystal panel comprising a picture element unit array and a microlens array.

However, Misawa et al. discloses a liquid crystal panel comprising a picture element unit array and a microlens array: the picture unit array having picture element units arranged two-dimensionally at a prescribed pitch on the substrate, three color picture elements, and a combination of a first and second picture elements being arranged in a first direction and another combination of the first and third color picture elements being arranged in a second direction

with the first color element common to both combinations; and the microlens array being arranged two-dimensionally above the picture element array at the pitch corresponding to the pitches of the two color picture element combinations arranged in the first and second direction on the substrate [see Figures 16-18; Column 15, Line 52 - Column 17, Line 34].

For the reasons set forward in the above rejection of claim 36, it would have been obvious to combine Lewis with Misawa et al. to obtain the invention as specified in claim 37.

Response to Arguments

5. Applicants' arguments filed September 27, 2002 have been fully considered but they are not persuasive. The applicants contend the prior art of Lewis (US 5,589,847) fails to disclose changing an initial sequencing order of the digital video data inputted through the input terminal into a different sequencing order, and for outputting the digital video data in the different sequencing order, as well as a selection circuit for selecting at least one of the signal transfer switches to output analog signals in the same order as the different sequencing order of the digital video data. However, the examiner respectfully disagrees. Lewis teaches changing an initial sequencing order of the digital video data [Fig. 15A, *serial* input digital data] inputted through the input terminal into a different sequencing order [Fig. 15A, *parallel* output digital data], and for outputting the digital video data in the different sequencing order, as well as a selection circuit [Fig. 15A, 520] for selecting at least one of the signal transfer switches [Fig. 15A, 550] to output analog signals in the same order as the different sequencing order of the digital video data (see Column 10, Lines 22-48). By such reasoning, the rejection of claims 1, 2, 4, 5, 7-19, 21, 22, 24-38, and 49-51 is deemed proper and thereby maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
February 5, 2003

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